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| Digital Isolation test report |
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| Table of content | Page |

1. Introduction 3

2. Digital inputs block diagram 3

3. DIGITAL OUTPUTS Block diagram 3

4. Measurements 4

4.1. Fiber-optic interface 4

4.2. Modulator Interface 5

4.3. PLC Interface 6

5. Conclusions 7

6. Glossary 8

7. references 8

Document Revision history 8

list of tables

**No table of figures entries found.**

list of Figures

Figure 1 - Digital Input block diagram 3

Figure 2 - Digital isolator block diagram 4

Figure 3 - Fiber-optic interface (pin-diode) 4

Figure 4 - Optocoupler to the Modulator 5

Figure 5 - Modulator Interface (response time) 5

Figure 6 - PLC interface 6

Figure 7 - PLC interface (response time) 6

# Introduction

This document aims to provide information about the response time of the D I/O isolation modules planned for digital I/O signals isolator.

Be aware this document does not intend to show the schematics of the circuits and the diagrams described below are only informative to be able to understand the interface and its connections.

# Digital inputs block diagram

The forward current in the input LED in the optocoupler should be controlled to 10mA, according to the supplier the maximum current allowed is 25mA, on the Figure 1. The RL limits the current to operate with TTL and 24VDC. This report does not include the response time evaluation of the digital inputs signals, but is important remark the LED status and digital input connections after the inverter.



Figure 1 - Digital Input block diagram

# DIGITAL OUTPUTS Block diagram

The digital outputs are driven by the MOSFET transistor to detect the cabling connection, then the signal can be used for the fiber-optic interface or the optocoupler for the PLC and the Modulator, both of them with different interface described below.



Figure 2 - Digital isolator block diagram

# Measurements

## Fiber-optic interface

CH1 (Yellow): 3V3 digital output. The total time measured from the digital output changes from high to low or normal state to interlock is 430ns. The CH3 (green) has been measured in the pin-diode board.

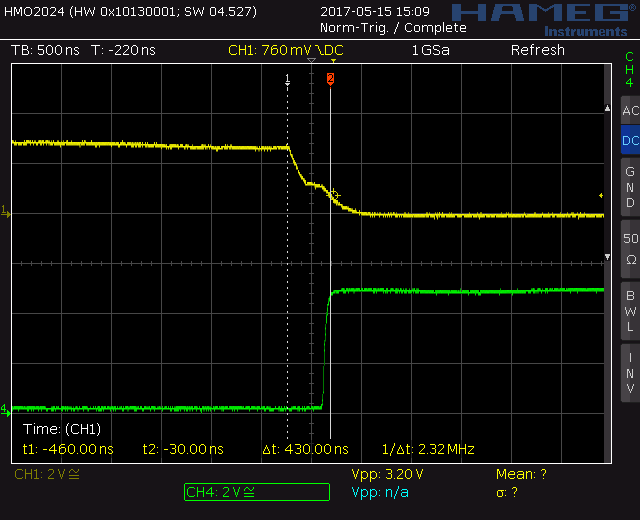


Figure 3 - Fiber-optic interface (pin-diode)

## Modulator Interface

The digital output of the conditioning board drives the ground signal of the Modulator, by default the input of the Modulator detects “1” from the pull-up resistor located internally in the Modulator. The total response or propagation time from the FPGA outputs (Figure 1) to the Modulator input simulated by a pull-up resistor of 1k @24VDC is 5.2us (Figure 4).



Figure 4 - Optocoupler to the Modulator

CH1 (Yellow): 3V3 digital output. The total time measured from the digital output changes from high to low or normal state to interlock is 5.2us. The CH3 (pink) has been measured in the resistor.

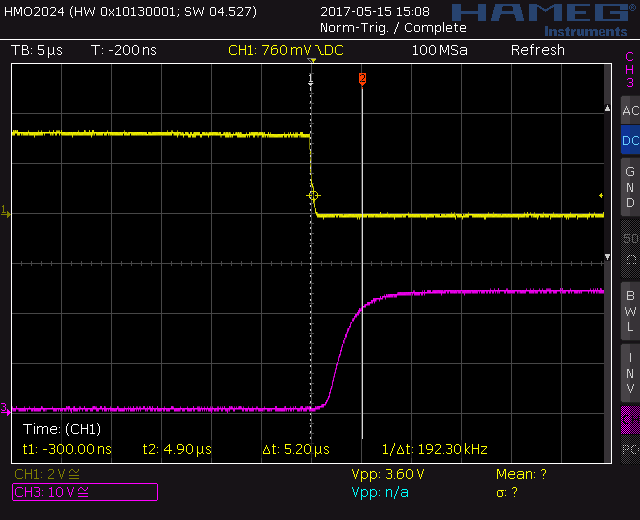


Figure 5 - Modulator Interface (response time)

## PLC Interface

Because the PLC does not require a fast reaction time, the interface might change a bit. The output of the signal conditioning board drives the 24VDC signal. The PLC includes an internal resistor to protect the I/O modules, then the signal does not need to be pulled-down.

The current measured was 7mA, therefore the resistor would be 3k4 in the PLC input (Figure 5). The response time would not be important as mentioned above, but the response time is quite fast despite the transitional time of the signal – 25us @24VDC.



CH1 (Yellow): 3V3 digital output. The total time measured from the digital output changes from high to low or normal state to interlock is ~25us. The CH3 (pink) has been measured in the PLC.

Figure 6 - PLC interface

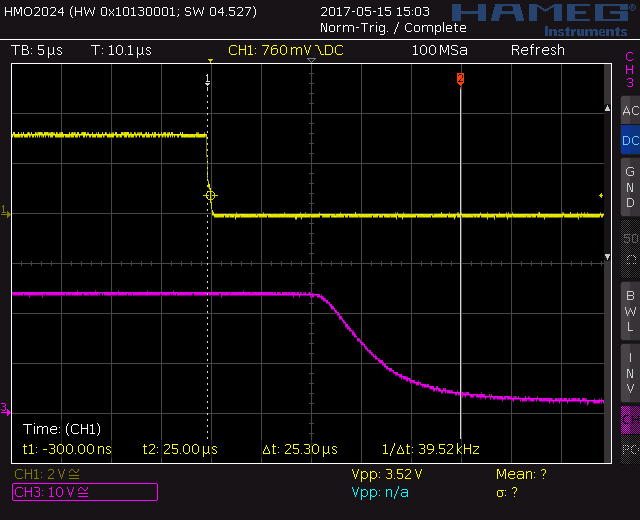


Figure 7 - PLC interface (response time)

# Conclusions

It is important to understand the function of the LED indicator, the main reason to install it was to know the status of the signal input/output. It is because the LED shall be connected to the inverter according to the behavior described (Figure 1 and 2).

All interfaces were previously tested in the lab with a dummy systems such as the Modulator, the PLC and pin-diode interfaces were tested with the equipment planned to use in the final design.

Keep in mind the tests did not include the same optocoupler and some minor changes of the connections of the inverter output.

# Glossary

| Term | Definition |
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# references

Document Revision history

| Revision | Reason for and description of change | Author | Date |
| --- | --- | --- | --- |
| 1 | First issue | Rafael | 2016-12-07 |
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